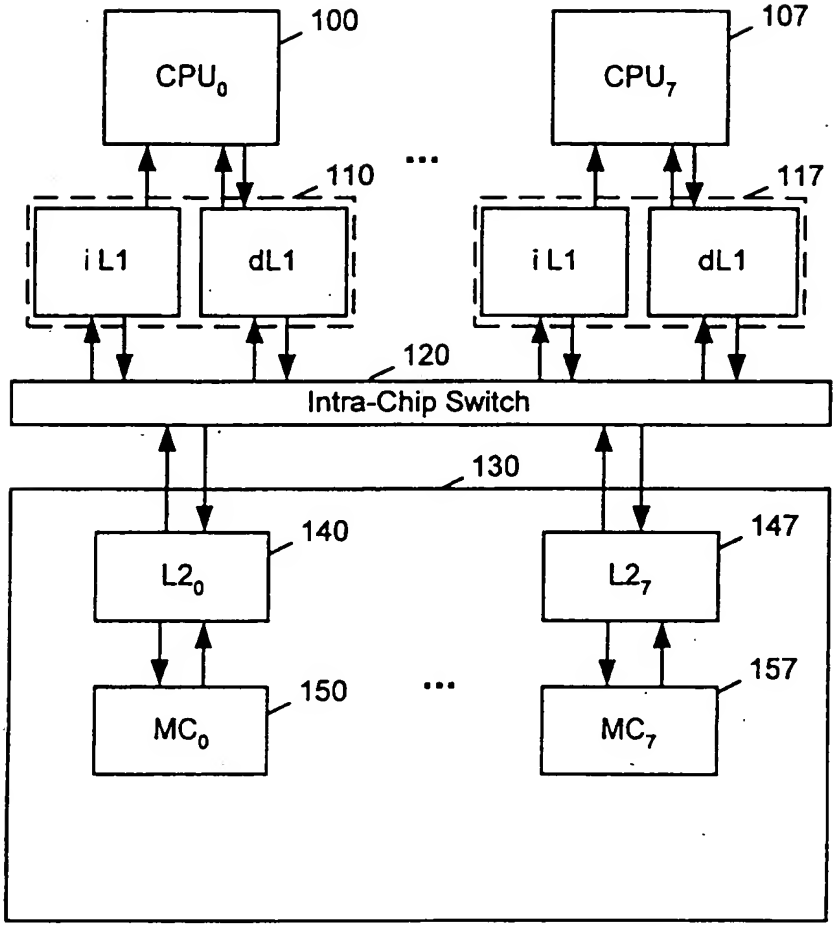
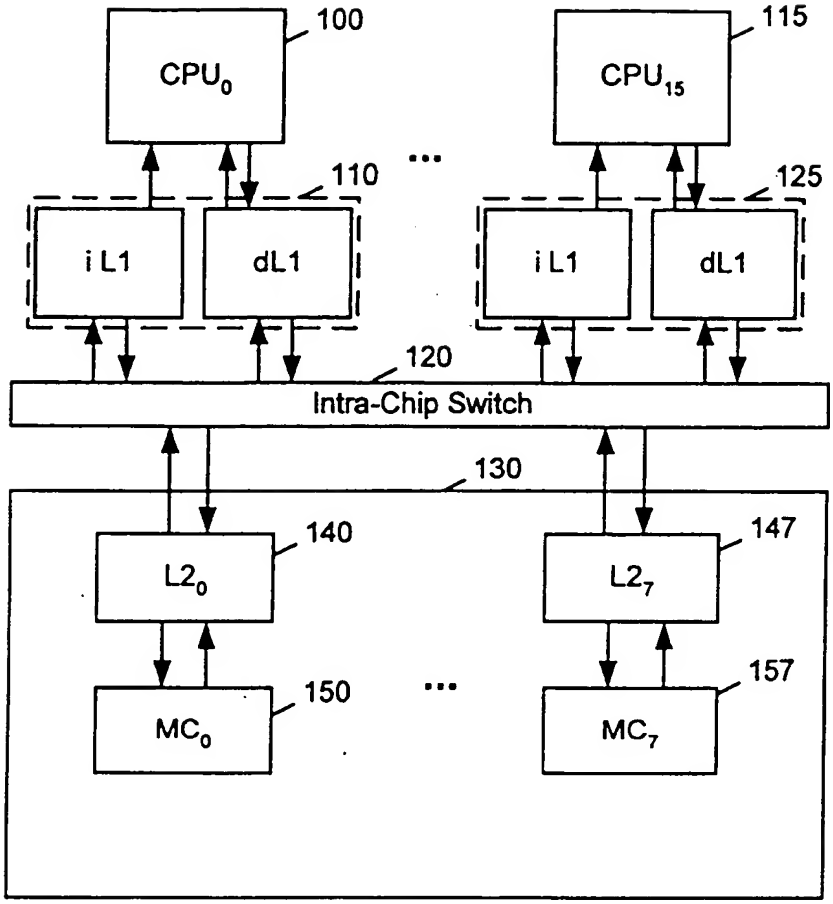

100
CPU0
107
CPU7
110
117
i L1
dL1
i L1
dL1
120
Intra-Chip Switch
130
140
L20
147
L27
150
MC0
157
MC7
10

Fig. 1


100
CPU0
115
CPU15
110
125
i L1
dL1
i L1
dL1
120
Intra-Chip Switch
130
140
L20
147
L27
150
MC0
157
MC7

20

Fig. 2

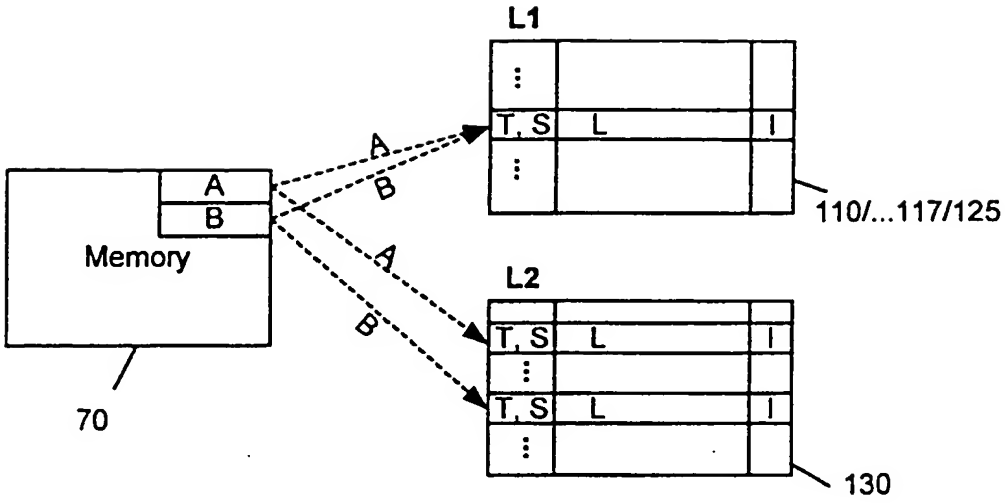


Fig. 5A

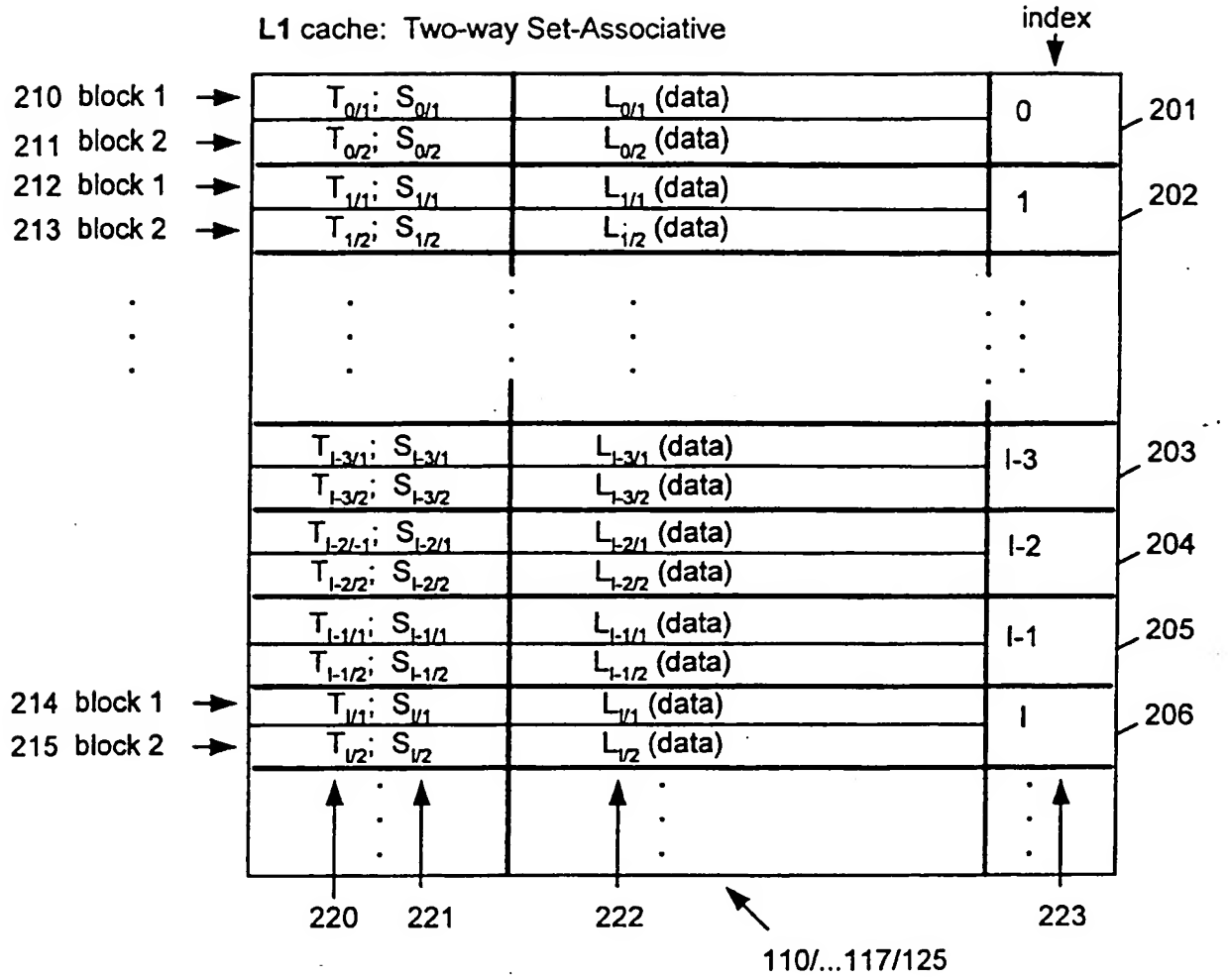
physical address: M bits (32/44/62)

t bits	i bits	m bits
Tag	Index (set mapping function)	Byte Select (offset w/in block)

301 302 303

30

Fig. 3



T=Tag
S=State

Fig. 4

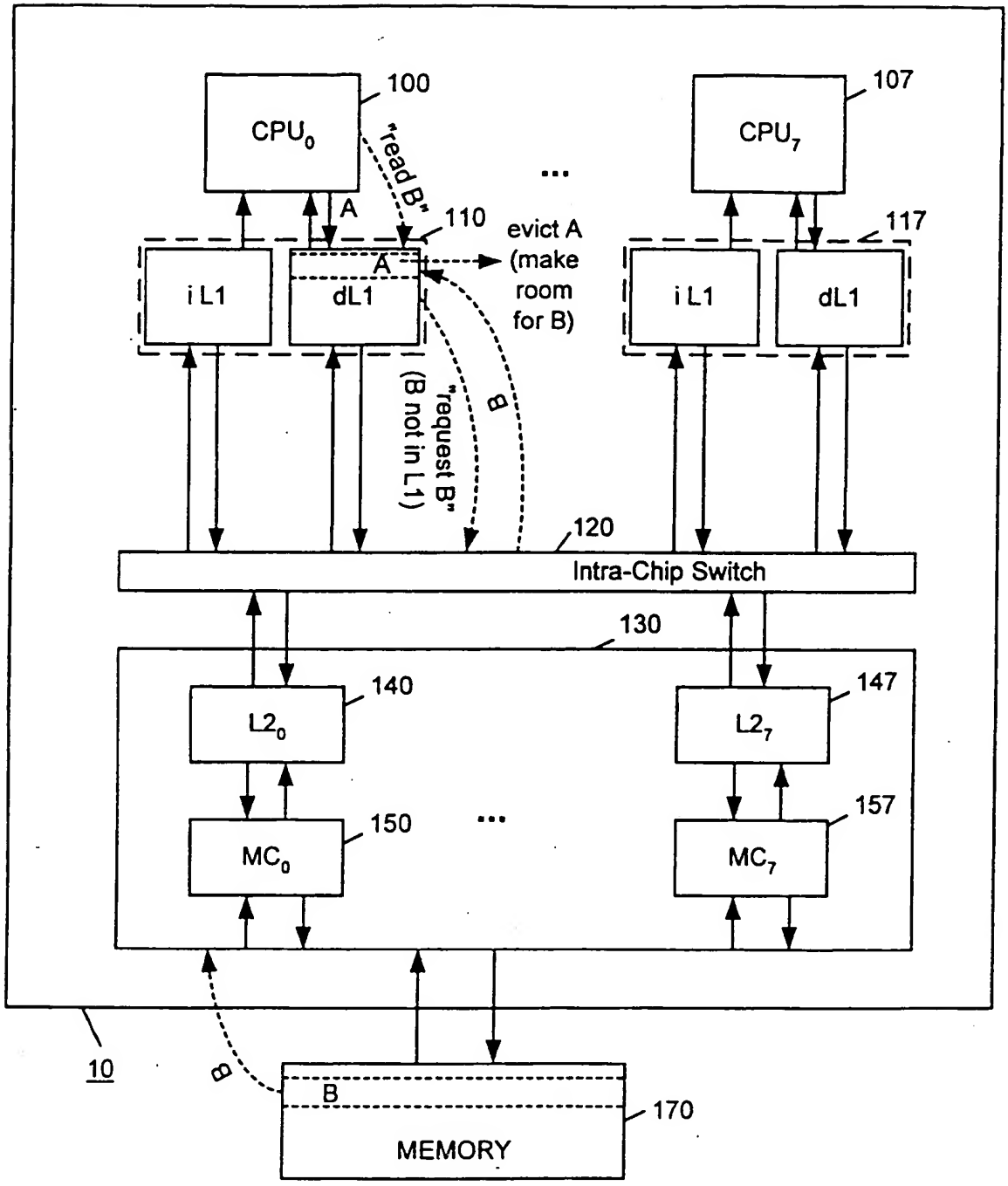
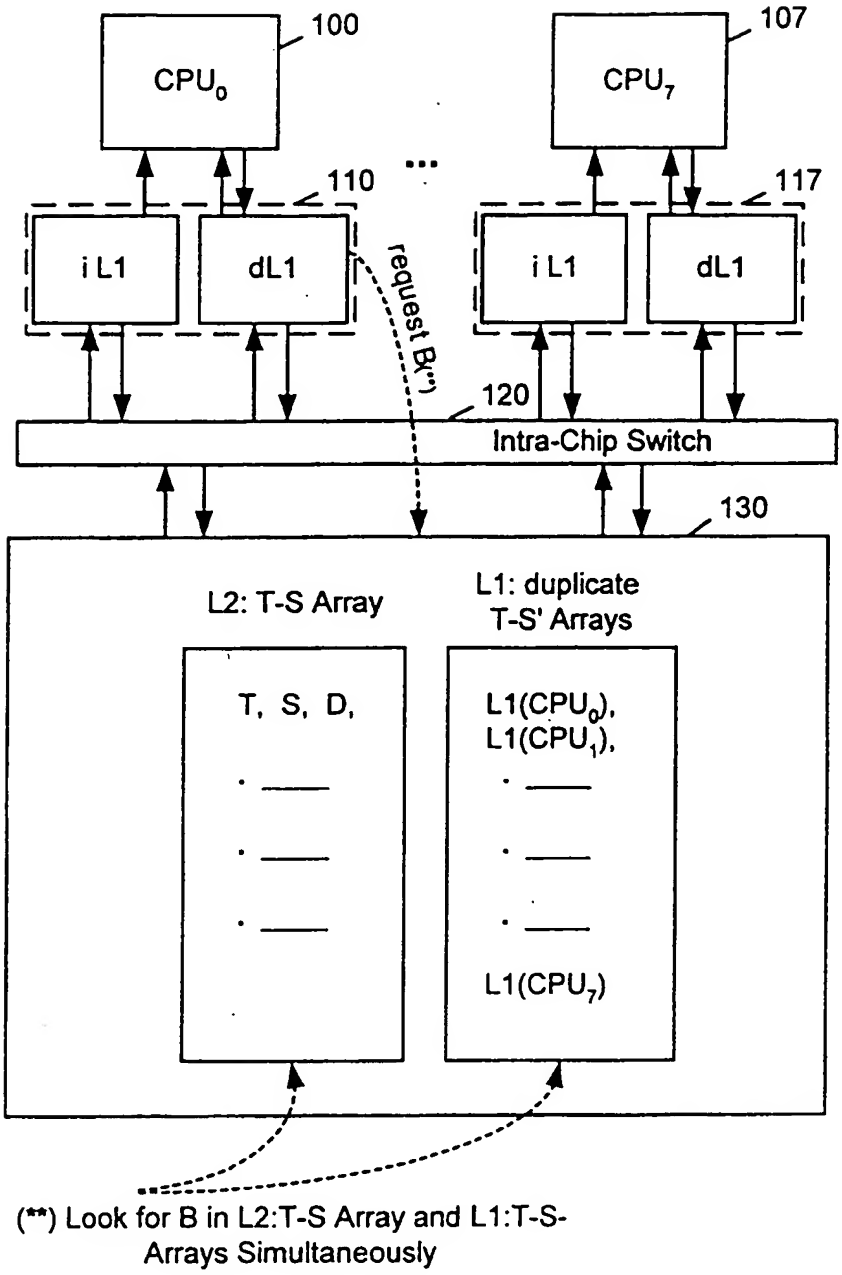

CPU0
100
"read B"
A
110
evict A
(make
room
for B)
A
iL1
dL1
"request B"
(B not in L1)
B
CPU7
107
117
iL1
dL1
120
Intra-Chip Switch
130
L20
140
L27
147
MC0
150
MC7
157
10
B
B
170
MEMORY

Fig. 5B


CPU0
100
CPU7
107
110
117
i L1
dL1
i L1
dL1
request B(**)
120
Intra-Chip Switch
130
L2: T-S Array
L1: duplicate
T-S' Arrays
T, S, D,
L1(CPU0),
L1(CPU1),
L1(CPU7)
(**) Look for B in L2:T-S Array and L1:T-S-
Arrays Simultaneously

10

Fig. 6

L2 Cache: Data Structure

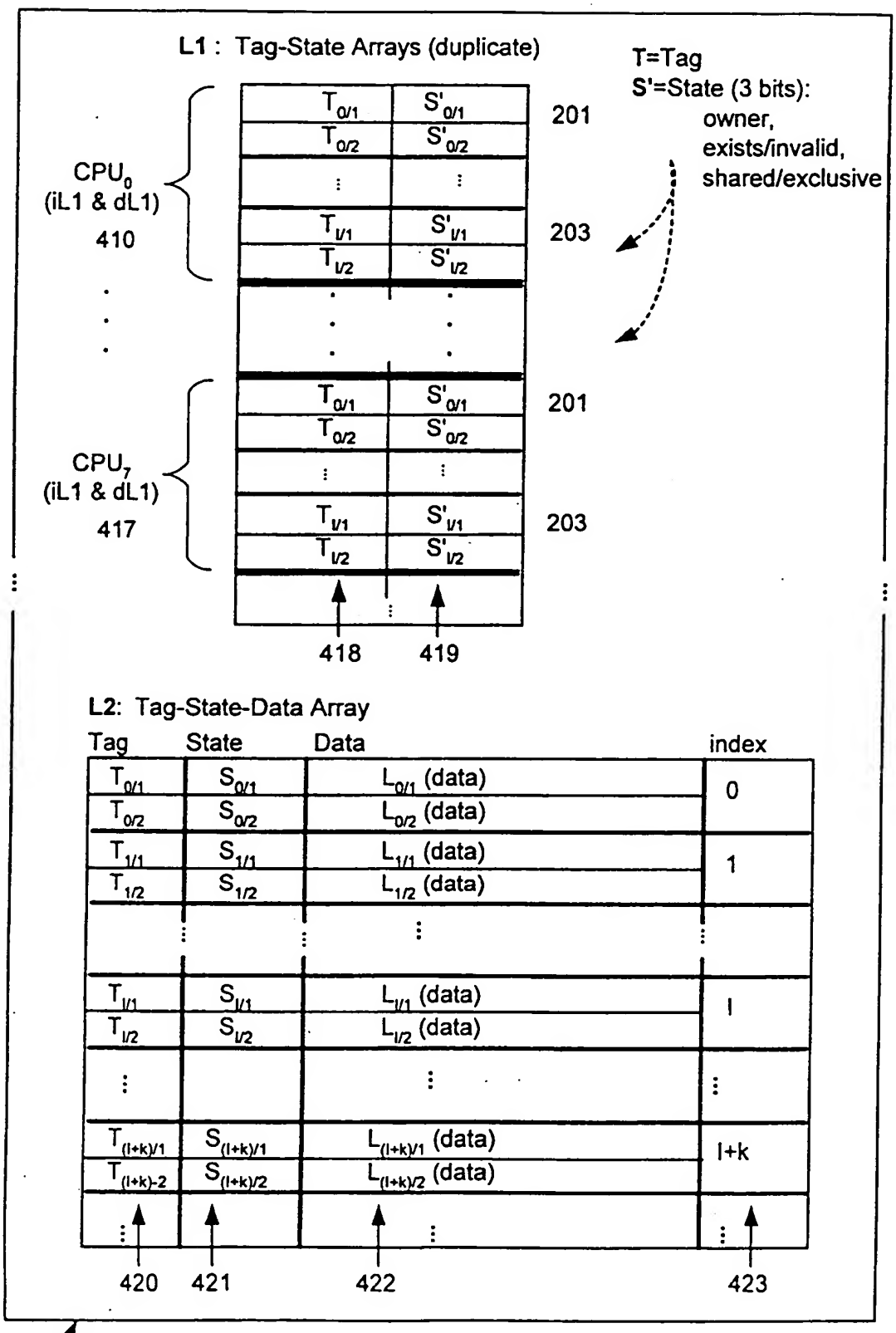


Fig. 7